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(54) INSULATION GATE TYPE FIELD EFFECT TRANSISTOR

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(72) Inventor: Tatehiro Okabe
c/o Central Research Institute, Hitachi, Ltd.
Kokubunji-shi, Higashi Koigakubo 1-chome, 280-ban

(72) Inventor: Kano Ochi
c/o Central Research Institute, Hitachi, Ltd.
Kokubunji-shi, Higashi Koigakubo 1-chome, 280-ban

(72) Inventor: Akira Yoshida
c/o Central Research Institute, Hitachi, Ltd.
Kokubunji-shi, Higashi Koigakubo 1-chome, 280-ban

(72) Inventor: Minoru Nagata
c/o Central Research Institute, Hitachi, Ltd.
Kokubunji-shi, Higashi Koigakubo 1-chome, 280-ban

(71) Applicant: Hitachi, Ltd.
Tokyo-to, Chiyoda-ku, Marunouchi 1-chome, 5-ban, 1-go

(74) Representative: Noritatsu Usuda, patent attorney

SPECIFICATIONS

1. Title of the Invention: Insulation Gate Type Field Effect Transistor

2. Scope of the Patent's Claims:

1. An insulation gate type of field effect transistor, characterized by the fact that it comprises a source and drain region of the second conductive type, formed at a reciprocal distance from a semiconductor substrate, which is of the first conductive type, wherein a gate electrode is located between said source and drain region so that it is deployed through an insulation film positioned at a distance from said drain region on the surface of said semiconductor substrate;

in an insulation gate type of field effect transistor having a low impurity layer of the second conductive type which reaches from said drain region to the channel region below said gate electrode;

wherein the impurity region of the second conductive type is deeper than said low impurity layer, having a higher impurity concentration than said low impurity layer, inside said low impurity layer in the vicinity of said drain area.

2. The insulation gate type of field effect transistor described in claim 1, characterized by the fact the when the dielectric constant of the semiconductor is expressed as e_s, the impurity concentration of said semiconductor as N the electricity amount (variable electricity) as q, and the real voltage drop in the drain junction is expressed as V_A, distance L between said impurity region and said drain region is characterized by the formula:

$$L \lesssim 2\left\{\frac{2\varepsilon_s}{qN_B}\cdot V_A\right\}^{\frac{1}{2}} \qquad (1)$$

3. The insulation gate type of field effect transistor described in claim 1, characterized by the fact that said drain region is surrounded by said source region, and also said low impurity layer and said low impurity region surround the entire periphery of said drain region.

4. The insulation gate type of field effect transistor described in claim 1, characterized by the fact that said impurity region is a region having an island shape deployed opposite one part of said drain region.

5. The insulation gate type of field effect transistor described in claim 1, characterized by the fact that said impurity region has the same degree of impurity concentration and of depth as said drain region.

Detailed Explanation of the Invention

(1) Sphere of Industrial Use

[page 2]

This invention relates to an insulation gate type of field effect transistor. More specifically, it relates to an insulation gate type of field effect transistor having a high pressure resistance, that is to say a high drain pressure resistance.

(2) Prior Art Technology

The insulation gate type of field effect transistors (hereinafter called simply MISFET) have been developed for devices requiring a high degree of integration density and a low power consumption and they are used mainly in IC for digital devices and as essential elements in LSI constructions. That is why the development aimed at improving the characteristics of MISFET devices was concentrated mainly on a design offering a high integration density and a low consumption of power, as well as a high-speed design. However, improvements relating to a pressure resistant design and a high output design have not bee satisfactory.

Incidentally, the main characteristics of MISFET, taken as a functional block, are related to the temperature coefficient applied to high input impedance, multiplication characteristics and the load of electric current. These characteristics are better displayed when they are applied to analog circuits. A high pressure resistant design of MISFET and a high output design thus present important problem areas for applicable use in analog circuits.

Figure 1 shows a known construction indicating the elements of a highly voltage resistant MISFIT design (D. M. Eib and H.G. Dill: IEDM 21 - 4 (1971).

The elements shown in Figure 1 represent a MISFET realized with a technology using ion implantation in an offset gate construction. As shown in Figure 1 which can be used to explain an example of the N-channel type, 11 is a P-type semiconductor substrate (impurity concentration in the range of $10^{14} \sim 10^{16}$ cm-^{3}), 12 and 13 are a source region, formed from a high concentration N-impurity type region, and a drain region (impurity concentration in the range of $10^{15} \sim 10^{21}$ cm-^{3}), respectively, 15 is a gate electrode, 16 and 17 are a source electrode and a drain electrode, respectively, and 18 is a gate insulation film. Number 14 indicates a low impurity concentration layer of the N-type, formed from drain 13 to the end part of gate electrode 15, which serves to relax the concentration in the electric field at the end part on the side of drain 13 of gate electrode 15, that is to say it is a low resistance layer (for example with an impurity concentration in the range of $1.5 \sim 2.5 \times 10^{12}/cm^{2}$). The construction containing these elements made it possible to increase more than 10 times the V value representing several hundred V, using more than 10 V and a low MISFET voltage (determined by the drain voltage resistance) of a MISFET according to prior art.

However, although the structural elements shown in Figure 1 make it possible to realize a highly resistance MISFET construction in the class of 300 V, these elements are not sufficiently resistant to a high voltage which is required for instance in a buffer MISFET construction used for a switching regulator, etc. Although a highly resistant MISFET construction that would have

a high value from the viewpoint of its use for industrial purposes requires a highly resistant construction design in the range of at least 400 ~ 600 V, the structure containing the elements shown in Figure 1 does not make it possible to realize such a highly voltage resistant design.

(3) Purpose of this Invention

The purpose of this invention is to realize a MISFET construction providing voltage resistance at least in the range of 400 ~ 600 V through an improved structural base of the conventional highly resistant MISFET structure shown in Figure 1.

(4) General Explanation of the Patent

The drain voltage resistance of MOSFET is limited by the field concentration in the inner part of the semiconductor in the vicinity of the end part of the gate electrode. At the same time, another limit is imposed by the PN junction voltage resistance of the semiconductor basic substance and of the drain region. The former problem can be resolved by the structure of elements which is shown in Figure 1, enabling to realize a highly resistant MISFET up to approximately 300 V. This invention makes it possible to realize a MISFET enabling a higher resistance of about 500 V through an improved PN junction resistance in the basic semiconductor substance and in the drain region.

In order to achieve this purpose, the MISFET of this invention uses an impurity region which is deeper than low resistance layer 14, preferably with an impurity region having the same concentration as the drain region, with a higher impurity concentration than in low resistance layer 14 having the same conductivity type in the vicinity of drain region 13 in low resistance layer 14.

In addition, the MISFET of this invention makes it possible to improve the drain resistance by creating a structure which surrounds the drain region by said impurity region of the same conductivity type as the drain which is deployed adjacent to the drain region in the low resistance layer, while drain region 13 is also surrounded by resistance layer 14.

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(Embodiments)

The following is an explanation of an embodiment of this invention which is based on the enclosed figures.

Figure 2 and Figure 3 are diagrams explaining an embodiment of the highly resistant MISFET of this invention. Figure 2 is a diagram showing a partial top view and figure 3 is a diagram showing a partial profile view of the construction. As shown in Figure 2 and 3, 1 indicates an N-type semiconductor substrate, 2 is a P-type source region, 3 is a P-type drain region, 5 is a p-type low impurity concentration region, 6 is a gate electrode, 7 and 8 are source

electrodes, 9 is an insulation film, and 9' is a gate insulation film. In this case, the voltage resistance of the PN junction formed by P-type drain 3 and N-type substrate 1 is determined by the circuit of edge part A of region 3 and its value is lower than the value of the voltage resistance of a PN junction that has a flat shape. Therefore, when a P-type impurity region 4 is formed and a suitable distance L is maintained between region 3 and region 4 as shown in Figure 2 and Figure 3, this makes it possible to relax the concentration of the electric field in the front end part A of region 3. In other words, during a status when a high drain voltage is applied, as long as a distance L is set so that a depletion layer is extending from region 3 and region 4 so that both are mutually associated, this makes it possible to prevent a breakdown in the front end part A of region A. Consequently, a high voltage design can be achieved. The formula which can be used as a criterion for distance L is indicated below.

$$L \lesssim 2\left\{\frac{2\varepsilon_s}{qN_B}\cdot V_A\right\}^{\frac{1}{2}} \qquad (1)$$

e_s: dielectric constant of the semiconductor,
N_B: semiconductor substrate impurity concentration,
q: electricity amount (variable electricity),
V_A: breakdown voltage in part A of a conventional construction which does not have region 4.

If for example, the following values of the P-channel MISFET shown in Figure 3 are used: impurity concentration in substrate 1 is expressed as $N_B = 5 \times 10^{14}$ cm^{-3}, the impurity concentration of source and drain areas 2 and 3 is expressed as $N_A = 1 \times 10^{19}$ cm^{-3}, the depth is 10 μm, the impurity concentration in low impurity concentration region 5 is expressed as $N_{AL} = 2 \times 10^{16}$ cm^{-3}, the depth is 0.5 μm, length 40 μm, the channel length is 10 μm when $V_A = 380$ V, the depth of region 4 is set to 10 μm, and the impurity concentration to 1×10^{19} cm^{-3}, and when length L = 14 μm, width l = 24 μm, a drain voltage resistance of 500 V will be obtained.

It is obvious that the above described region 4 made it possible to improve resistance by more than 30% when compared to the drain resistance of a MISFET which does not have the above described region. Since region 4 which was used in the embodiment shown is Figure 2 and Figure 3 is deployed in a ring shape only in 1 location so as to surround drain region 3, this also makes it possible to assure a better drain resistance.

Figure 4 is a diagram explaining another embodiment of this invention. Since the peripheral length of the gate will be long in a MISFET construction characterized by a high voltage and a large current, the inter-digital type of construction which is shown in Figure 4 is used. As shown in Figure 4, drain region 3 has an oblong, rectangular projecting part 3', which means that its width C will be narrow. When region 3' is formed using impurity diffusion, etc., with a similar pattern shape, due to the shape of the front end part B, the electric field concentration in part B will be very significant, causing a deterioration of the voltage resistance. If the diffusion depth of the impurity is shallow, or if width C is narrow, this will also have a very

significant influence. Therefore, when region 3' having the same conductive type is formed as shown in Figure 4, this makes it possible to relax the concentration of the electric field in part B, enabling to improve resistance.

Distance L between region 3' and region 4' can be obtained according to the same formula (1) which is used in the embodiment above. Also in this embodiment, when the MISFET shown in Figure 4 is used while the impurity concentration of N-type Si substrate 1 is expressed as N_B = 5 x 10^{14} cm^{-3}, the impurity concentration of P-type region 3' is expressed as N_A = 1 x 10^{14} cm^{-3}, width C = 14 μm, and the depth is 10 μm, V_A = 340 V; when the impurity concentration of region 4' is 1 x 10^{18} cm^{-3}, the depth is 10 μm, L = 10 μm, and when l = 24 μm, a drain voltage of 420 V will be obtained.

As was explained above, the invention can be utilized to improve voltage resistance between the semiconductor substrate and the drain of a MISFET having high voltage resistance.

The following is an explanation of an example of an N-channel element according to the high voltage resistance manufacturing method of this invention.

As shown in Figure 5 (A), oxide film 9 (made of SiO_2, etc.), which is 130 nm thick, is formed on P-type silicon substrate 1. On top of that is formed a polysilicon film having a thickness of 450 nm. Since the resistance of the polysilicon layer will be high during this status, ion implantation is conducted from the surface by implanting ions in 2 x 10^{14} locations/cm^2, and annealing is applied for 30 minutes by using a temperature of about 1,000°C.

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Next, etching is applied to remove the required part except for the part creating the gate electrode in which polysilicon 6 is left. This is the status shown in Figure 5 (A). Next, in order to form the N-type low impurity layer for the highly resistant design, ions of phosphorus are implanted in oxide film 9 and N^- type region 5 is formed. At this point, when acceleration voltage is 130 keV, ion implantation is applied with a ion dose of 2 x 10^{13} locations/cm^2. Next, an SiO^2 film is formed with a thickness of 800 nm according to the CVD (Chemical Vapor Deposition) method and the SiO_2 film is removed with the exception of location 10 as required for a diffusion mask. (See Figure 5 (B)). Next, N-type regions 2, 3 and 4 are formed with an impurity concentration of 1 x 10^{20} cm^{-3}, having a depth of 25 μm according to a common heat diffusion method to create an impurity source $POCl_2$. (See Figure 5 (C)). Region 2 is formed as the source area, region 3 as the drain area, and region 4 is formed in an island shape between the source and the drain. Next, SiO_2 film 10 is removed, another SiO_2 film containing phosphorus is formed again with a thickness of 800 nm, and a window is created in the contact part of the source and drain to create an Al electrode. These processes can be used without any change for various types of common semiconductor devices. The profile structure of the elements obtained in this manner is identical to the structure shown in Figure 3.

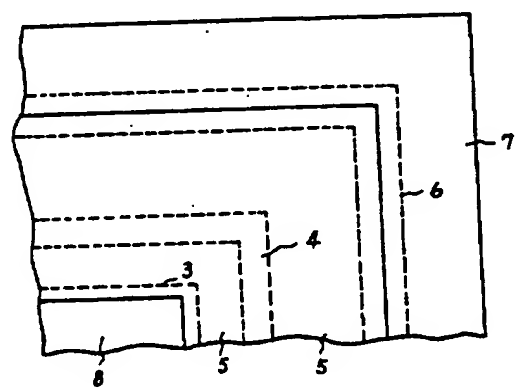
Brief Explanation of Figures

Figure 1 shows a profile view of the construction of a MISFET according to prior art, Figure 2 shows a partial top view of the a part containing the elements of Embodiment 1 of a MISFET according to this invention, Figure 3 is a partial profile view showing elements of Embodiment 1 of a MISFET according to this invention, Figure 4 is a partial top view showing the elements of Embodiment 2 of a MISFET according to this invention, and Figure 5 is a profile view showing the elements of an example of the manufacturing process of a MOSFET according to this invention.

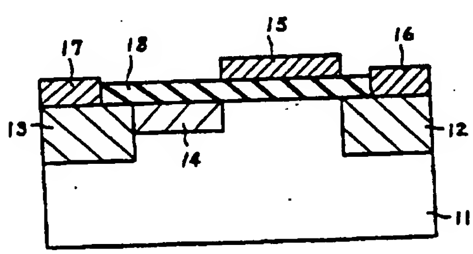
1 ... semiconductor substrate, 2 ... source region, 3 ... drain region, 4 ... impurity region having the same conductivity type as the drain region, 5 ... low impurity concentration region (resistance layer), 6 ... gate electrode, 7 ... source electrode, 8 ... drain electrode, 9 ... insulation film, 9' ... gate insulation film.   Representative: Noritatsu Usuda, Patent Atorney.

(Figure 1, Figure 2, and Figure 3)

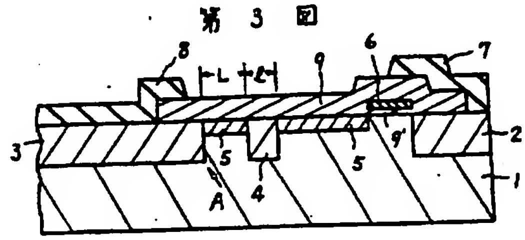
第 2 図



第 1 図



第 3 図



(Figure 4 and Figure 5)

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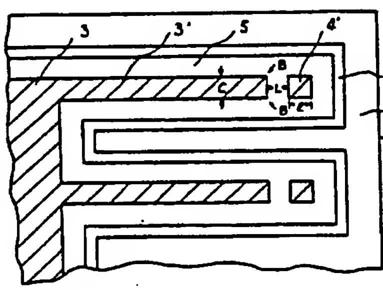
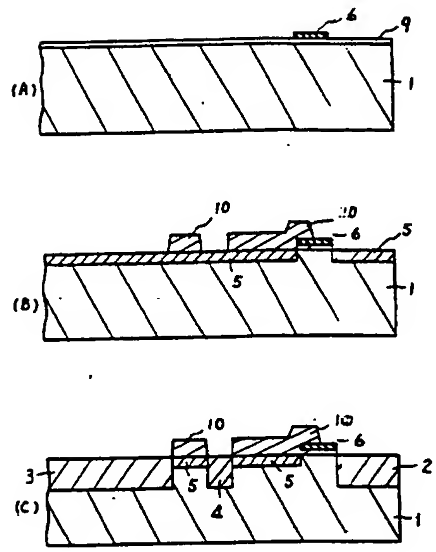
第 5 図

第 4 図





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⑭絶縁ゲート形電界効果トランジスタ

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⑫発 明 者 岡部健明
国分寺市東恋ヶ窪1丁目280番地株式会社日立製作所中央研究所内
⑫発 明 者 越智鹿之
国分寺市東恋ヶ窪1丁目280番地株式会社日立製作所中央研究所内
⑫発 明 者 吉田功
国分寺市東恋ヶ窪1丁目280番地株式会社日立製作所中央研究所内
⑫発 明 者 永田穣
国分寺市東恋ヶ窪1丁目280番地株式会社日立製作所中央研究所内
⑪出 願 人 株式会社日立製作所
東京都千代田区丸の内1丁目5番1号
⑭代 理 人 弁理士 薄田利幸

明 細 書

発明の名称 絶縁ゲート形電界効果トランジスタ

特許請求の範囲

1．第1導電形の半導体基体に互いに離れて形成された第2導電形のソース、ドレイン領域と、該ソース、ドレイン領域間の前記半導体基体表面上の前記ドレイン領域から離れた位置に絶縁膜を介して設けられたゲート電極と、前記ドレイン領域から前記ゲート電極下のチャンネル領域に到達する第2導電形の低不純物層とを有する絶縁ゲート形電界効果トランジスタにおいて、前記ドレイン領域に近接して前記低不純物層内に、前記低不純物層の不純物濃度より高く、前記低不純物層より浅い第2導電形の不純物領域を設けてなることを特徴とする絶縁ゲート形電界効果トランジスタ。

2．前記基体の半導体の誘電率をε_s、前記基体の不純物濃度をN、電気量をq、ドレイン接合の実質降伏電圧をV_Bとしたとき、前記不純物領域と前記ドレイン領域との距離Lは、

$$L \leq 2\left\{\frac{2\varepsilon_s}{qN}\cdot V_B\right\}^{\frac{1}{2}}$$

であることを特徴とする特許請求の範囲第1項記載の絶縁ゲート形電界効果トランジスタ。

3．前記ドレイン領域は前記ソース領域に囲まれてなり、前記低不純物層、前記不純物領域も前記ドレイン領域の全周を囲むことを特徴とする特許請求の範囲第1項記載の絶縁ゲート形電界効果トランジスタ。

4．前記不純物領域は前記ドレイン領域の一部に対向して設けられた島状領域であることを特徴とする特許請求の範囲第1項記載の絶縁ゲート形電界効果トランジスタ。

5．前記不純物領域は前記ドレイン領域と同程度の不純物濃度、深さを有することを特徴とする特許請求の範囲第1項記載の絶縁ゲート形電界効果トランジスタ。

発明の詳細な説明

(1) 発明の利用分野

本発明は、絶縁ゲート形電界効果トランジスタに関している。さらに詳しくは、本発明は高耐圧、すなわち高ドレイン耐圧の絶縁ゲート形電界効果トランジスタに関するものである。

(2) 従来技術

絶縁ゲート形電界効果トランジスタ（以下、MISFET と略称）は、高集積密度、低消費電力デバイスとして、これまで主にデジタル用IC，LSIの構成要素として発展してきた。そのためMISFET の特性向上の開発は、主として高集積密度、低消費電力化、さらに高速化が中心に進められ、高耐圧化、高出力化に関しては十充分な改良がなされていない。

ところで、MISFET 単体としての性能上の主な特長は、高入力インピーダンス、自乗特性、電流の負の温度係数を有している点にある。これ等の特長は、MISFET のアナログ回路への応用において、より発揮できるものである。アナログ回路に適用する場合、MISFET の高耐圧化、高出力化が重要な問題点である。

高耐圧MISFET としては、第1図に示す素子構造が知られている（D. M. Erb and H. G. Dill : IEDM21－4（1971））。

第1図の素子は、オフセットゲート構造とイオン打込み技術を用いて高耐圧化を実現したMISFET である。第1図において、Nチャンネル形を例にとつて説明すれば、11はP形半導体基板（不純物濃度10^{14}～10^{16} cm^{-3}）、12および13はそれぞれ高濃度N形不純物領域からなるソース、およびドレイン領域（不純物濃度10^{19}～10^{21} cm^{-3}）、15はゲート電極、16および17はそれぞれソース電極およびドレイン電極、18はゲート絶縁膜である。14はゲート電極15のドレイン13側の端部における電界の集中を緩和し、ドレイン耐圧を高め素子の高耐圧化を実現するために、ドレイン13からゲート電極15の端部まで延びて形成されたN形の低不純物濃度層、すなわち抵抗層である（例えば不純物濃度1.5～2.5×10^{12}/cm^2）。この素子構造により、従来たかだか数十Vと低いMISFET の

耐圧（ドレイン耐圧によつて決つていた）を数百Vと十倍以上高めることができた。

しかしながら、第1図の素子構造により、300Vクラスの高耐圧MISFET を実現できたが、スイッチング・レギュレータ等に用い得るパワーMISFET としては、まだ十分な高耐圧素子とはなつていない。産業上の利用価値の高い高耐圧MISFET としては、400～600V以上の高耐圧化を達成する必要があるが、第1図の素子構造のままでは、これ程の高耐圧化を実現することはできない。

(3) 発明の目的

本発明は、第1図に示した従来の高耐圧MISFET の構造をベースにした上で、さらに改良を加えることにより、400～600V、又はそれ以上の耐圧を有するMISFET を実現することを目的とするものである。

(4) 発明の総括説明

MISFET のドレイン耐圧は、ゲート電極端付近の半導体基体内部の電界集中により制限されるとともに、ドレイン領域と半導体基体間のPN接合耐圧によつても制限を受ける。前者は第1図の素子構造により解決され、300V程度の高耐圧MISFET が実現できる。本発明は、さらに、後者のドレイン領域と半導体基体間のPN接合耐圧を改善することにより、500V程度もしくはそれ以上の高耐圧MISFET を実現するものである。

かかる目的を達成するため、本発明のMISFET においては、第1図のMISFET において、抵抗層14中のドレイン領域13の近傍に、ドレイン領域と同一導電形で、抵抗層14よりも不純物濃度の高い、好ましくはドレイン領域と同程度の不純物濃度で、抵抗層14よりも深い不純物領域を設けることを骨子とする。

さらに、本発明のMISFET においては、抵抗層14によつてドレイン領域13を囲むとともに、該抵抗層中にドレイン領域に近接して設けられたドレインと同一導電形の上記不純物領域によつてドレイン領域をとり囲む構造をとることによつて、ドレイン耐圧を一層向上させることができる。

(5) 実施例

以下、本発明を実施例を参照して詳細に説明する。

第2図，第3図は本発明の高耐圧MISFET の実施例を説明するための図面で、第2図は部分平面図、第3図は部分断面構造図である。第2図，第3図において、1はN形半導体基板、2はP形ソース領域、3はP形ドレイン領域、5はP形低不純物濃度領域、6はゲート電極、7，8は各々ソース電極、ドレイン電極、9は絶縁膜、9′はゲート絶縁膜である。ここでP形ドレイン3とN形基板1で形成されるPN接合の耐圧は、領域3の先端A部の曲率により決まり、その値は平面状PN接合耐圧の値よりも低くなつている。そこで第2図，第3図に示すように、P形不純物領域4を形成し、領域3と領域4間の距離Lを適当に設計すれば、領域3の先端部Aの電界集中を緩和することができる。つまりドレインに高電圧が印加された状態において、領域3および領域4から延びる空乏層が互いに交わるように距離Lを設定す

れば、領域3の先端A部での降伏は防ぐことが出来、従つて高耐圧化が達成される。ここで距離Lの目安として(1)式を示す。

$$L \lesssim 2\left\{\frac{2\,\varepsilon_s}{q\,N_B}\cdot V_A\right\}^{\frac{1}{2}} \qquad (1)$$

ε_s ：半導体の誘電率

N_B ：半導体基板不純物濃度

q ：電気量

V_A ：領域4が無い従来構造におけるA部の降伏電圧

例えば、第2，3図のPチャンネルMISFETで、基板1の不純物濃度 $N_B = 5\times10^{14}\,cm^{-3}$、ソース・ドレイン領域2，3の不純物濃度 $N_A = 1\times10^{19}\,cm^{-3}$、深さ10 μm、低不純物濃度層5の不純物濃度 $N_{AL} = 2\times10^{16}\,cm^{-3}$、深さ0.5 μm、長さ40 μm、チャンネル長10 μmの時 $V_A = 380$ Vであり、領域4の深さを10 μm、不純物濃度を $1\times10^{19}\,cm^{-3}$ として、距離L＝14 μm、幅 ℓ＝24 μmとしたとき、ドレイン耐圧500Vが得られた。もちろん、本発明

で述べた領域4が無い場合のMISFET のドレイン耐圧は380Vで、本発明によつて30％以上の耐圧改善が可能となつた。第2，3図の実施例では、領域4は、ドレイン領域3を囲む様に環状に1ケだけ設けたが、これを2重，3重と増していけば、さらにドレイン耐圧が改善されることも確認されている。

第4図は、本発明の他の実施例を説明するための図である。高耐圧、大電流MISFET では、ゲート周辺長を大きくするため、第4図に示すようなインターディジタル形構造が採用される。第4図において、ドレイン領域3は、3′のように長方形の張出し部分があり、その幅Cも狭くなつている。このようなパターン形状を有する領域3′を不純物の熱拡散などで形成すると、先端部Bの形状の為、B部の電界集中が著しく、耐圧劣化の原因となる。不純物の拡散深さが浅い場合、あるいは幅Cが狭い場、この影響は著しい。そこで第4図に示すように、領域3′と同一導電形の領域4′を形成すれば、B部の電界集中を緩和し、耐

圧を改善することが可能である。領域3′と領域4′との距離Lは、前実施例と同様に(1)式で与えられる。本実施例においても、N形Si基板1の不純物濃度 $N_B = 5\times10^{14}\,cm^{-3}$、P形領域3′の不純物濃度 $N_A = 1\times10^{14}\,cm^{-3}$、幅C＝14 μm、深さ10 μmの第4図に示したMISFETの時、$V_A = 340$ Vであり、領域4′の不純物濃度 $1\times10^{19}\,cm^{-3}$、深さ10 μmでL＝10 μm, ℓ＝24 μmのとき、ドレイン耐圧420Vが得られた。

以上述べたように、本発明は高耐圧MISFETのドレイン、基板間耐圧の改善に利用できる。

以下、本発明の高耐圧MISFET の製造方法をNチャンネル素子を例にとり示す。

第5図（A）に示す様に、P形シリコン基板1に130nm厚の酸化膜（SiO_2 等）9を形成し、その上にポリシリコン膜を450nmの厚さに形成する。このままではポリシリコン層の抵抗は高いので、表面からりんイオンを 2×10^{16} ケ/cm^2 打込んで、約1000℃×30分間のアニ

ールを行う。次にゲート電極となるべき部分のポリシリコン6を残して、他をエッチングで除去する。この状態を第5図（A）に示す。次に高耐圧化の為のN形低不純物濃度層を形成する為、りんイオンを酸化膜9を通して打込み、N^-形領域5を形成する。この時の加速電圧は130keVで、打込まれたイオンドーズは2×10^{11}ケ/cm^2である。次に高温（650℃）にて、CVD（Chemical Vapor Deposition）法によりSiO_2膜を800nmの厚さに形成し、拡散のマスクとなるべき場所10を残して、他のSiO_2膜を除去する。（第5図（B））。次に、不純物源を$POCl_3$とする通常の熱拡散法によつて、2.5μmの深さに不純物濃度$1\times10^{20}cm^{-3}$のN形領域2，3，4を形成する（第5図（C））。領域2はソース、領域3はドレイン、領域4はソース・ドレイン間の島領域として働く。次にSiO_2膜10を除去し、再びりんを含んだSiO_2膜を800nmの厚さに形成し、ソースとドレインのコンタクト部分の窓あけをし、Al

電極を形成する。これらの工程は通常の半導体デバイスと何ら異なる点はない。こうして得られた素子の断面構造は、第3図と同じとなる。

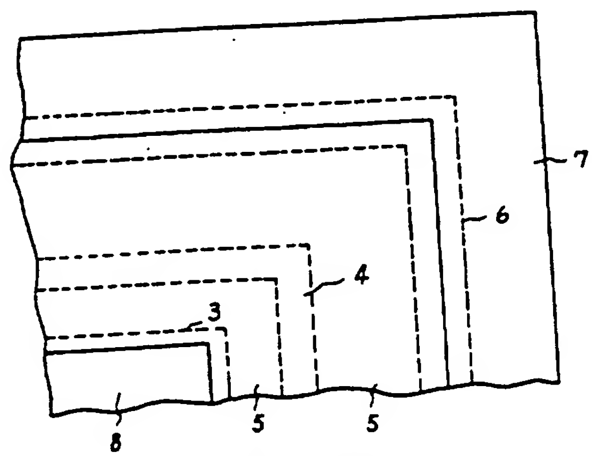
図面の簡単な説明

第1図は従来のMISFETの構造を示す断面図、第2図は本発明のMISFETの第1の実施例の素子を示す部分平面図、第3図は本発明のMISFETの第1の実施例の素子を示す部分断面図、第4図は本発明のMISFETの第2の実施例の素子を示す部分平面図、第5図は本発明のMISFETの製造工程の一例を示す素子断面図である。

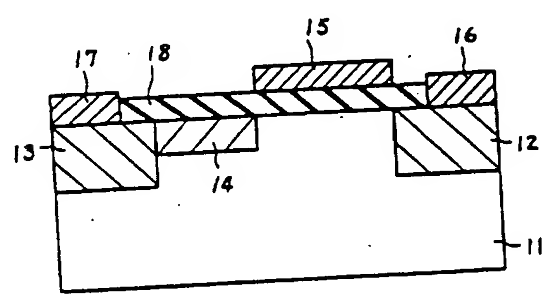
1…半導体基板、2…ソース領域、3…ドレイン領域、4…ドレイン領域と同一導電形の不純物領域、5…低不純物濃度領域（抵抗層）、6…ゲート電極、7…ソース電極、8…ドレイン電極、9…絶縁膜、9′…ゲート絶縁膜。

代理人　弁理士　薄田利幸

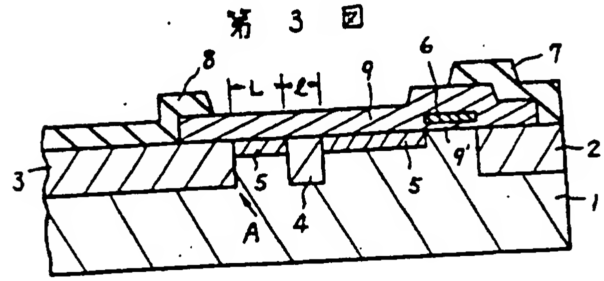
第2図



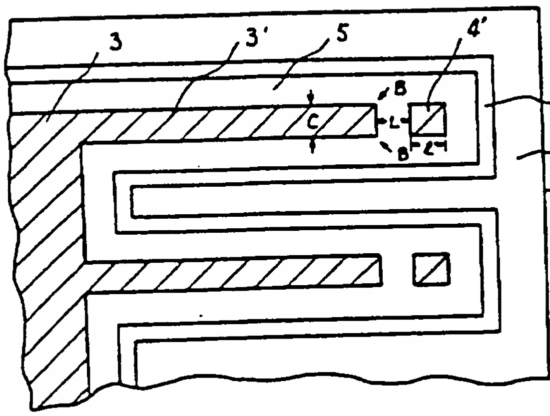
第1図



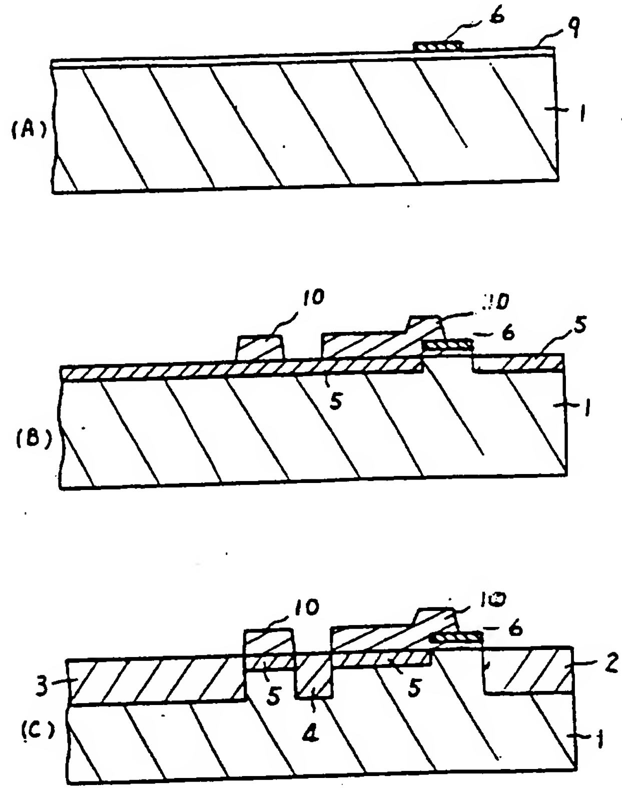
第3図



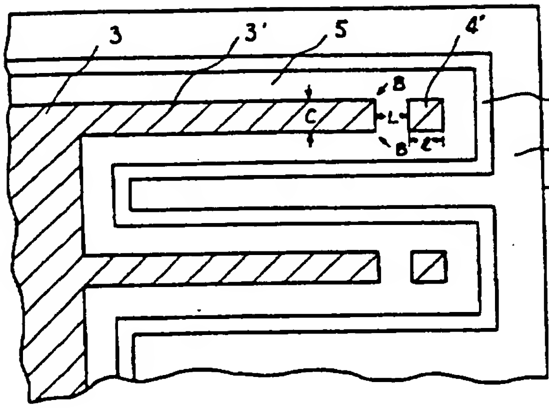
第 4 図



第 5 図



第 4 図



第 5 図